

High Q Reference Oscillator for High Performance Radar Waveform Generator

PhD Student: Estevan Chia Hung TU

Thesis Director: Jean-Baptiste BEGUERET (IMS)

Thesis Co-Director: Emmanuel PISTONO (TIMA)

Co-Supervisor: Stephane THURIES (NXP)

CIFRE Thesis with the company NXP Semiconductors France and the laboratory *Intégration du Matériau au Système (IMS)*, as part of the *École doctorale des Sciences Physiques et de l'Ingénieur (SPI)*, since January 2023. It is also in collaboration with the laboratory Techniques of Informatics and Microelectronics for Integrated Systems (TIMA).

Abstract

To meet the demand for next generation radar transceiver and improve their performances, a new generation of FMCW chirp generator must be developed. An architecture based on low-frequency DDS should fulfil such requirement, and this PhD focuses on one of its main part: a very low phase noise clock generator.

The objective of this work is to study the feasibility of the project in order to propose and design architectures for clock generation, based on high quality factor frequency resonator. The performances of this system will need to respect the defined specifications, with the oscillator's phase noise as one of the major parameters.

Market and bibliographic researches was conducted, by taking account of crucial parameters, to decide the sort of resonator which will be used and the oscillator architectures that can be implemented with it.

It was identified that piezoelectric resonators are the most suitable to achieve the aimed performances at the desired resonance frequency and still keeping a high quality factor.

Two principal topologies of a voltage controlled oscillator (VCO) were considered for the design: Cross-Coupled Oscillator and Differential Colpitts Oscillator. Both will be designed, validated through simulation, fabricated, tested and measured in laboratory. Additionally their performances will be compared. Only differential structures were taken into account as they are less sensible to common mode noises.

The g_m/I_D methodology is used as the core design technique to accurately size the transistors, in accordance with the aimed current and the transconductance needed for oscillation, and linked to the concept of noise, as it is one of the main concerns, in order to reduce its impact to the circuit. As well, the design will be conducted to decrease major phase noise contributors, such as flicker and thermal noises.

Cadence Virtuoso is the main software used, as it contains all the libraries, simulation environments, transistor technologies and tools required to accomplish this work.